Notice of Allowability	Application No.	Applicant(s)	
	10/651,839	BICSAK ET AL.	
	Examiner	Art Unit	
	Todd Ingberg	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *11/3/06*.

2. ☒ The allowed claim(s) is/are *1-15*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *11/27/06* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

TODD INGBERG
PRIMARY EXAMINER

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Francis Maquire on November 27, 2006.

The application has been amended as follows:

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Claim 1

A method for execution on a signal processing unit for constructing a control flow graph from a computer executable program the instructions of which belong to one or more computer architecture instruction sets, said method comprising defining a number of block leader types including at least one type related to an instruction set change, block leaders specifying basic block boundaries in the program, said basic blocks including instructions or data, building a control flow graph structure comprising basic blocks found in the program, adding control flow and addressing information to said control flow graph by propagating through said basic blocks and internals **of said basic blocks** [thereof] .

Claim 13

A system for constructing a control flow graph from a computer executable program, the instructions of which belong to one or more computer architecture instruction sets, said system comprising a processing device and a memory device for processing and storing instructions and data, and a data transfer device for accessing data, said system arranged to define a number of block leader types including at least one type related to an instruction set change, block leaders specifying basic block boundaries in the program, said basic blocks including instructions or data, said system further arranged to build a control flow graph structure comprising basic blocks found in the program, and to add control flow and addressing information to said control flow graph by propagating through said basic blocks and internals **of said basic blocks and stored on said memory device** [thereof].

Claim 15

A system for constructing a control flow graph from a computer executable program, the instructions of which belong to one or more computer architecture instruction sets, said system comprising a processing means and a memory means for processing and storing instructions and data, and a data transfer device for accessing data, said system arranged to define a number of

block leader types including at least one type related to an instruction set change, block leaders specifying basic block boundaries in the program, said basic blocks including instructions or data, said system further arranged to build a control flow graph structure comprising basic blocks found in the program, and to add control flow and addressing information to said control flow graph by propagating through said basic blocks and internals **of said basic blocks and stored on said memory device** [thereof].

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Claim 1

A method for execution on a signal processing unit for constructing a control flow graph from a computer executable program the instructions of which belong to one or more computer architecture instruction sets, said method comprising defining a number of block leader types including at least one type related to an instruction set change, block leaders specifying basic block boundaries in the program, said basic blocks including instructions or data, building a control flow graph structure comprising basic blocks found in the program, adding control flow and addressing information to said control flow graph by propagating through said basic blocks and internals of said basic blocks and stored on said memory device.

Claim 13

A system for constructing a control flow graph from a computer executable program, the instructions of which belong to one or more computer architecture instruction sets, said system comprising a processing device and a memory device for processing and storing instructions and data, and a data transfer device for accessing data, said system arranged to define a number of block leader types including at least one type related to an instruction set change, block leaders specifying basic block boundaries in the program, said basic blocks including instructions or data, said system further arranged to build a control flow graph structure comprising basic blocks found in the program, and to add control flow and addressing information to said control flow graph by propagating through said basic blocks and internals of said basic blocks and stored on said memory device.

Claim 15

A system for constructing a control flow graph from a computer executable program, the instructions of which belong to one or more computer architecture instruction sets, said system comprising a processing means and a memory means for processing and storing instructions and data, and a data transfer device for accessing data, said system arranged to define a number of block leader types including at least one type related to an instruction set change, block leaders specifying basic block boundaries in the program, said basic blocks including instructions or data, said system further arranged to build a control flow graph structure comprising basic blocks found in the program, and to add control flow and addressing information to said control flow graph by propagating through said basic blocks and internals of said basic blocks and stored on said memory device .

REASONS FOR ALLOWANCE

2. The following is an examiner's statement of reasons for allowance:

The invention has an aspect of reverse engineering from an executable to intermediate forms (CFG). Reverse engineering is a field of its own. One example is USPN # 6,061,513 Scandura where the executable is reverse back to intermediate form Abstract Syntax Trees (ASTs), which in compiler theory is the step prior to Control Flow Graphs. Scandura then allows a user to select which programming language to generate source code. Scandura actually reverses from an executable to far to meet the limitations of the claimed invention and Scandura does not roll forward supporting another instruction set architecture.

In terms of prior art that performs retargeting several references that teach retargeting compilers are of record. One is USPN #5,920,721 Hunter who among other teachings teaches generation from source to multiple versions of an instruction set architecture. The source to executable (rolling forward) is the traditional approach to producing an executable.

Skidmore USPN #5,488,714 processes source code modules for the sake of source code conversion. Clearly Skidmore does not start with an excecutable.

The closest prior art of record is USPN # 5,918,035 Van Praet et al, who generates retargeted code from a simulator. Column 3, lines 1 to 16 state "the model is an instruction level simulator" and "... all code generation phases find the information they need in the model without any analysis needed." the claimed invention the model is the existing executable and analysis is required to extract the required structures CFG and data.

The claimed invention also mentions the space to incorporate retargeting information (data structure) during the operation. The Examiner in an effort to determine if a de facto

standard for such as layout existed reviewed HMDES Version 2.0 Specification and the MOVE framework.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Correspondence Information

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Todd Ingberg whose telephone number is (571) 272-3723. The examiner can normally be reached on during the work week..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Todd Ingberg
Primary Examiner
Art Unit 2193

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